LOW-POWER CAN TRANSCEIVER WITH BUS WAKE-UP

FEATURES

- **Improved Drop-in Replacement for the TJA1040**
- **±12 kV ESD Protection**
- **Low-Current Standby Mode with Bus Wake-up: 5 μA Typical**
- **Bus-Fault Protection of –27 V to 40 V**
- **Rugged Split-Pin Bus Stability**
- **Dominant Time-Out Function**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance with Low V_{CC}**
  - **Monotonic Outputs During Power Cycling**
- **DeviceNet Vendor ID # 806**

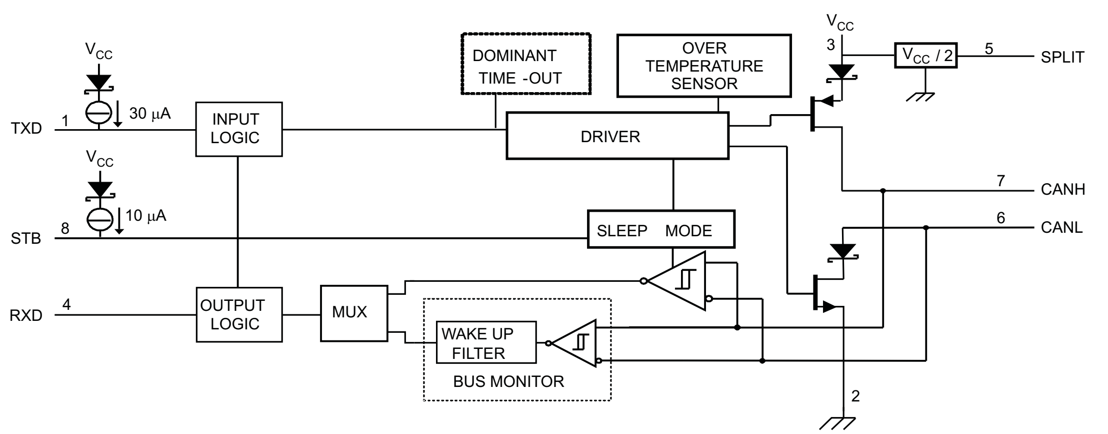
APPLICATIONS

- **Battery Operated Applications**
- **Hand-Held Diagnostics**
- **Medical Scanning and Imaging**
- **HVAC**
- **Security Systems**
- **Telecom Base Station Status and Control**
- **SAE J1939 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**
- **Industrial Automation**
  - **DeviceNet™ Data Buses**

DESCRIPTION

The SN65HVD1040 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). As CAN transceivers, these devices provide differential transmit and receive capability for a CAN controller at signaling rates of up to 1 megabit per second (Mbps). (1)

Designed for operation in especially harsh environments, the device features ±12 kV ESD protection on the bus and split pins, cross-wire, overvoltage and loss of ground protection from –27 to 40 V, overtemperature shutdown, a –12 V to 12 V common-mode range, and will withstand voltage transients from –200 V to 200 V according to ISO 7637.



(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (Continued)

The STB input (pin 8) selects between two different modes of operation; high-speed or low-power mode. The high-speed mode of operation is selected by connecting STB to ground.

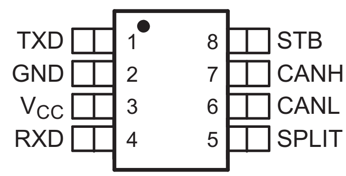
If a high logic level is applied to the STB pin of the SN65HVD1040, the device enters a low-power bus-monitor standby mode. While the SN65HVD1040 is in the low-power bus-monitor standby mode, a dominant bit greater than 5 μs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

A dominant-time-out circuit in the SN65HVD1040 prevents the driver from blocking network communication during a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

The SPLIT output (pin 5) is available on the SN65HVD1040 as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network.

The SN65HVD1040 is characterized for operation from –40°C to 125°C.

SN65HVD1040



ORDERING INFORMATION

PART NUMBER	DOMINANT TIME-OUT	LOW-POWER BUS MONITOR	PACKAGE(1)	MARKED AS	ORDERING NUMBER
SN65HVD1040	YES	YES	SOIC-8	VP1040	SN65HVD1040D (rail)
					SN65HVD1040DR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

			VALUE
V_{CC}	Supply voltage(2)		–0.3 V to 7 V
$V_{I(bus)}$	Voltage range at any bus terminal (CANH, CANL, SPLIT)		–27 V to 40 V
$I_{O(OUT)}$	Receiver output current		-20 mA to 20 mA
	Voltage input, transient pulse(3), (CANH, CANL, SPLIT)		–200 V to 200 V
ESD	Human Body Model	Bus terminals and GND	±12 kV
	Human body model (4)	All pins	±4 kV
	Charged-device-model(5)	All pins	±1 kV
	Machine model		±200 V
V_I	Voltage input range (TXD, STB)		–0.5 V to 6 V
T_J	Junction temperature		–55°C to 170°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6 & 7.
(4) Tested in accordance JEDEC Standard 22, Test Method A114-A.
(5) Tested in accordance JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12(1)		12	V
V_{IH}	High-level input voltage	TXD, STB	2		5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0		0.8	V
V_{ID}	Differential input voltage		–6		6	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			2	
t_{SS}	Maximum pulse width to remain in standby				0.7	µs
T_J	Junction temperature		–40		150	C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current, V_{CC}	Dominant	V_I = 0 V, 60 Ω Load, STB at 0 V		50	70	mA
		Recessive	V_I = V_{CC}, STB at 0 V		6	10	
		Standby	STB at VCC, VI = VCC		5	12	µA

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	STB at 0 V, See Figure 9	90		230	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive		90		230	

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 1 and Figure 2	2.9	3.4	4.5	V
		CANL		0.8		1.75	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3 V, STB at 0 V, See Figure 1 and Figure 2	2	2.5	3	V
V_O	Bus output voltage (Standby)		R_L = 60 Ω, STB at V_{CC}, See Figure 1 and Figure 2	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 1 and Figure 2, and Figure 3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 1 and Figure 2	1.4		3	
V_{SYM}	Output symmetry (Dominant or Recessive) [$V_{O(CANH)} + V_{O(CANL)}$)		STB at 0 V, See Figure 2 and Figure 13	0.9×V_{CC}	V_{CC}	1.1×V_{CC}	V
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3 V, R_L = 60 Ω, STB at 0 V, See Figure 1 and Figure 2	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No Load	–0.5		0.05	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		STB at 0 V, See Figure 8	2	2.3	3	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3		
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	μA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	μA
$I_{O(off)}$	Power-off TXD Leakage current		V_{CC} at 0 V, TXD at 5 V			1	μA
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL Open, See Figure 12	–120	–72		mA
			V_{CANH} = 12 V, CANL Open, See Figure 12		0.36	1	
			V_{CANL} = –12 V, CANH Open, See Figure 12	–1	–0.5		
			V_{CANL} = 12 V, CANH Open, See Figure 12		71	120	
C_O	Output capacitance		See Input capacitance to ground in *RECEIVER ELECTRICAL CHARACTERISTICS*.				

(1) All typical values are at 25 C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V, See Figure 4	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low-level output		25	45	120	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)				25	
t_r	Differential output signal rise time			25		
t_f	Differential output signal fall time			50		
t_{en}	Enable time from silent mode to dominant	See Figure 7			10	μs
t_{dom}	Dominant time-out	See Figure 10	300	450	700	μs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	High-speed mode	STB at 0 V, See Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage	High-speed mode	STB at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})	High-speed mode	STB at V_{CC}	100	125		mV
V_{IT}	Input threshold voltage	Standby mode	STB at V_{CC}	500		1150	mV
V_{OH}	High-level output voltage		I_O = –2 mA, See Figure 6	4	4.6		V
V_{OL}	Low-level output voltage		I_O = 2 mA, See Figure 6		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current		CANH or CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			5	µA
$I_{O(off)}$	Power-off RXD leakage current		V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground, (CANH or CANL)		TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		20		pF
C_{ID}	Differential input capacitance		TXD at 3 V, V_I = 0.4 sin (4E6πt)		10		pF
R_{ID}	Differential input resistance		TXD at 3 V, STD at 0 V	30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)		TXD at 3 V, STD at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] x 100%		$V_{CANH} = V_{CANL}$	–3%	0%	3%	

(1) All typical values are at 25 C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	STB at 0 V, TXD at 3 V, See Figure 6	60	100	130	ns
t_{pHL}	Propagation delay time, high-to-low-level output	STB at 0 V, TXD at 3 V, See Figure 6	45	70	130	ns
t_r	Output signal rise time	STB at 0 V, TXD at 3 V, See Figure 6		8		ns
t_f	Output signal fall time	STB at 0 V, TXD at 3 V, See Figure 6		8		ns
t_{BUS}	Dominant time required on bus for wake-up from standby(1)	STB at V_{CC} Figure 11	0.7		5	µs

(1) The device under test shall not signal a wake-up condition with dominant pulses shorter than t_{BUS} (min) and shall signal a wake-up condition with dominant pulses longer than t_{BUS} (max). Dominant pulses with a length between t_{BUS} (min) and t_{BUS} (max) may lead to a wake-up.

SPLIT-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3×V_{CC}	0.5×V_{CC}	0.7×V_{CC}	V
$I_{O(stb)}$	Standby mode leakage current	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

STB-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	STB at 2 V	–10		0	µA
I_{IL}	Low level input current	STB at 0 V	–10		0	µA

PARAMETER MEASUREMENT INFORMATION

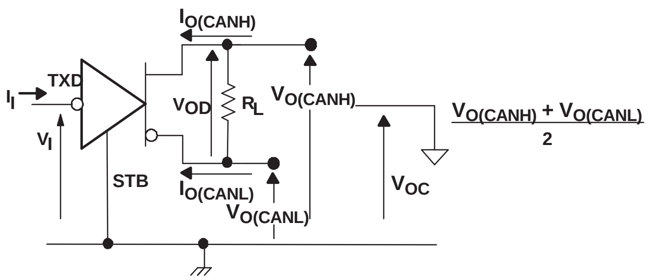


Figure 1. Driver Voltage, Current, and Test Definition

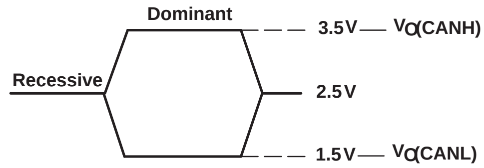


Figure 2. Bus Logic State Voltage Definitions

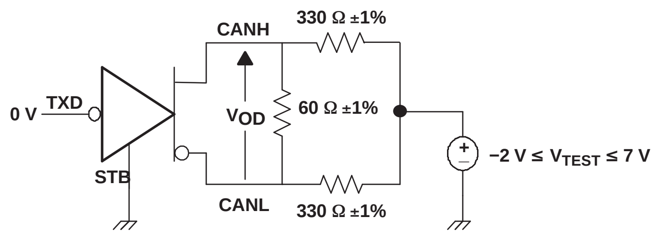


Figure 3. Driver V_{OD} Test Circuit

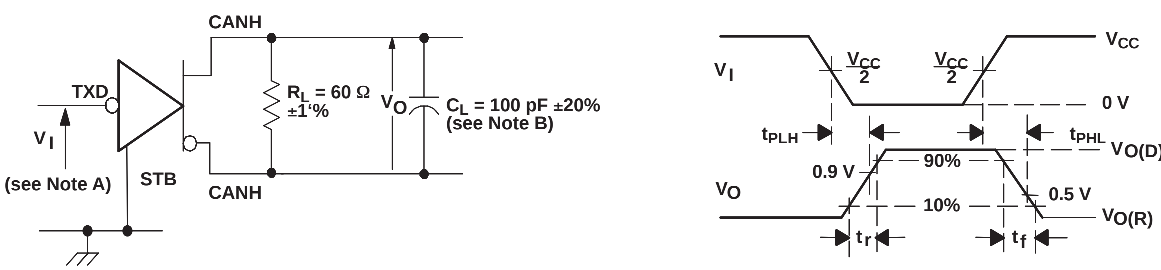


Figure 4. Driver Test Circuit and Voltage Waveforms

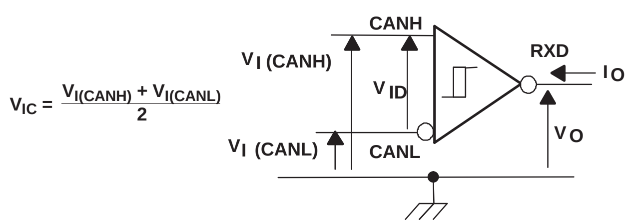
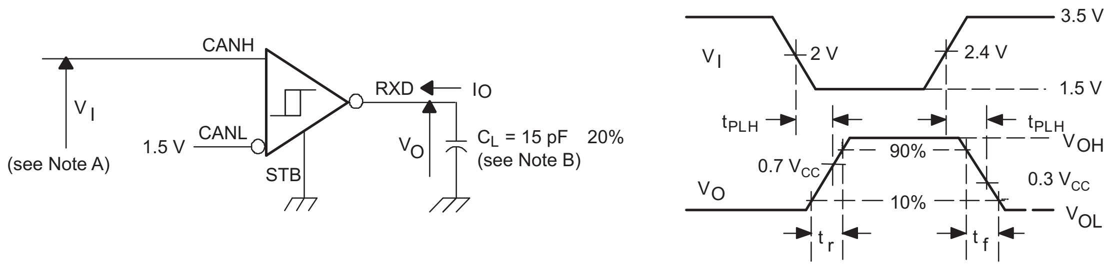


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within 20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

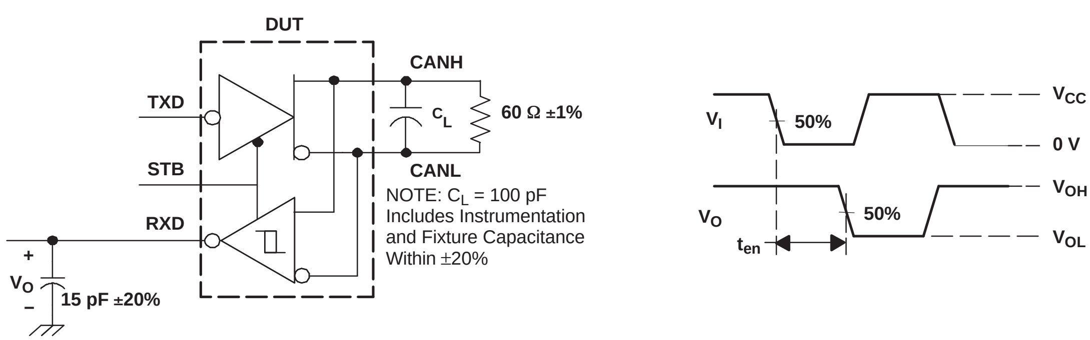
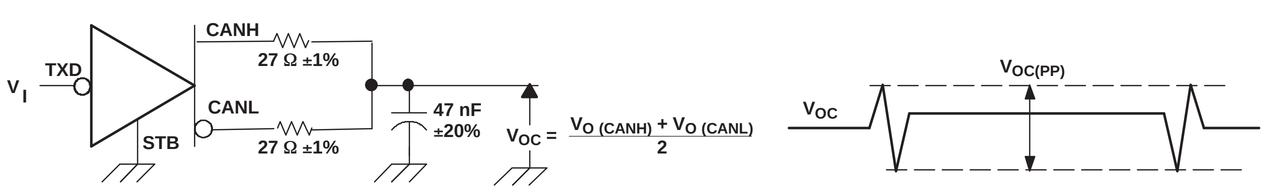
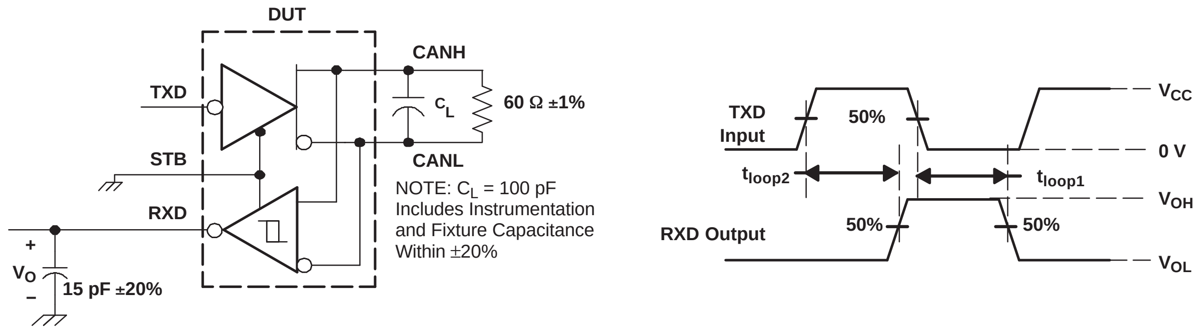


Figure 7. t_{en} Test Circuit and Voltage Waveforms



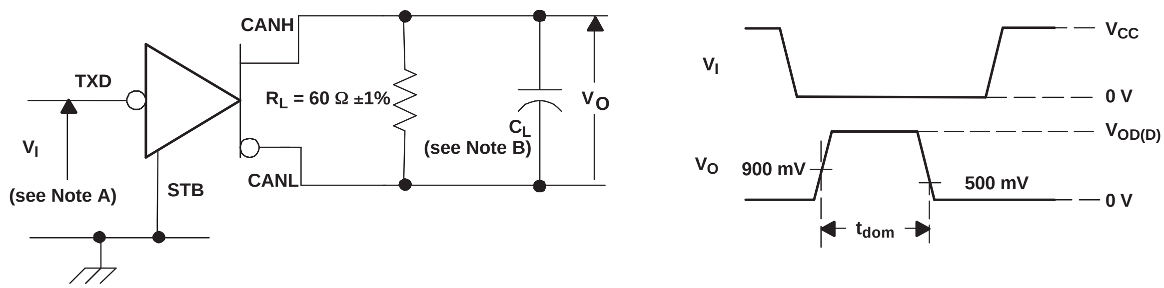
A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Peak-to-Peak Common Mode Output Voltage Test and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

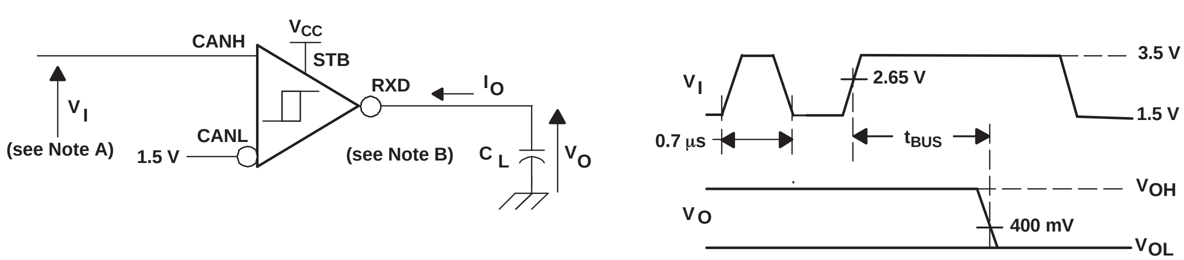
Figure 9. t_{loop} Test Circuit and Voltage Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within 20%.

Figure 10. Dominant Time-Out Test Circuit and Waveform



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_II bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics; t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 50 Hz, 30% duty cycle.

B. C_L = 15 pF includes instrumentation and fixture capacitance within 20%.

Figure 11. t_{BUS} Test Circuit and Waveform

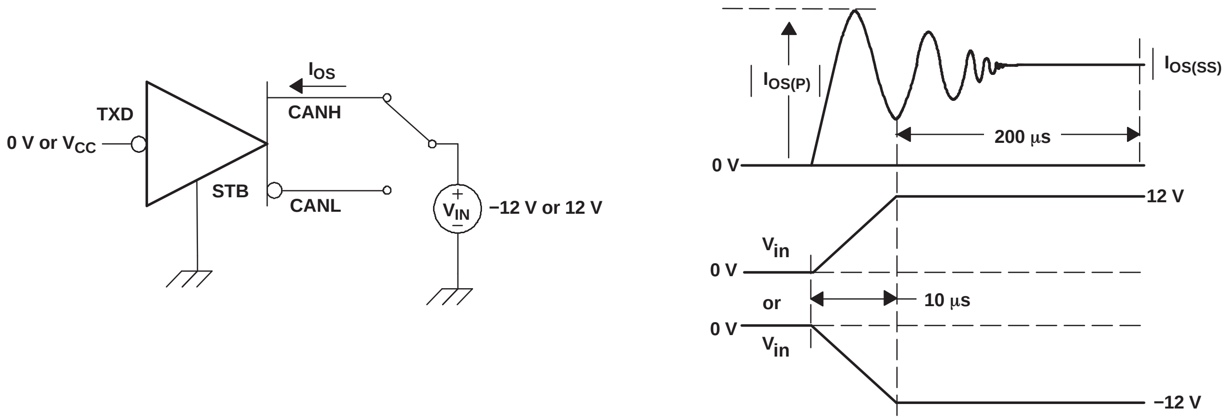


Figure 12. Driver Short-Circuit Current Test and Waveform

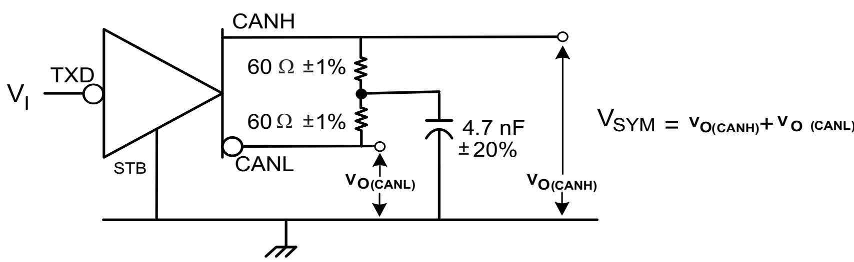


Figure 13. Driver Output Symmetry Test Circuit

DEVICE INFORMATION

Table 2. DRIVER FUNCTION TABLE[(1)]

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	DOMINANT
H	L	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H or Open	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; Z = high impedance

Table 3. RECEIVER FUNCTION TABLE[(1)]

DIFFERENTIAL INPUTS V_{ID} = CANH - CANL	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq$ 0.9 V	L	L	DOMINANT
$V_{ID} \geq$ 1.15 V	H or Open	L	DOMINANT
0.5 V < V_{ID} < 0.9 V	X	?	?
$V_{ID} \leq$ 0.5 V	X	H	RECESSIVE
Open	X	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal Resistance, Junction-to-Air	Low-K Thermal Resistance[(1)]		211		°C/W
		High-K Thermal Resistance		131		°C/W
θ_{JB}	Thermal Resistance, Junction-to-Board			53		°C/W
θ_{JC}	Thermal Resistance, Junction-to-Case			79		
P_D	Device Power Dissipation	R_L = 60 Ω, S at 0 V, Input to TXD a 500kHz 50% duty-cycle square wave		112	170	mW
T_{JS}	Junction Temperature, Thermal Shutdown [(2)]			190		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.
(2) Extended operation in thermal shutdown may affect device reliability, see the *Application Information* section.

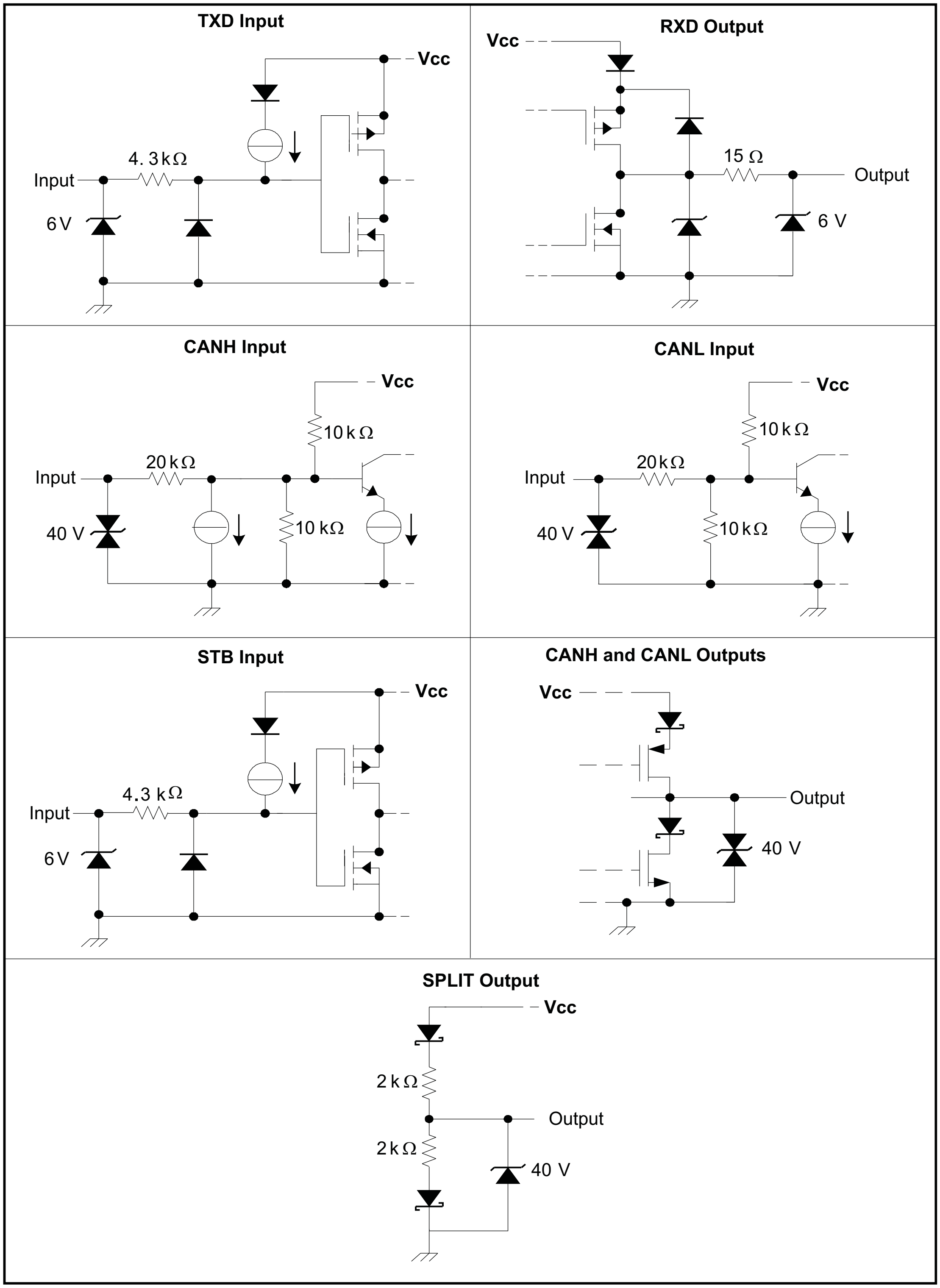
DEVICE INFORMATION

Table 4. Parametric Cross Reference With the TJA1040

TJA1040[1]	PARAMETER	HVD10xx
	TJA1040 DRIVER SECTION	
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
	TJA1040 BUS SECTION	
$V_{th(dif)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{hys(dif)}$	Differential input hysteresis	Receiver V_{hys}
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{O(dif0(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(def)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
$C_{i(cm)}$	Input capacitance to ground	Receiver C_{I}
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
	TJA1040 RECEIVER SECTION	
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
	TJA1040 SPLIT PIN SECTION	
V_{O}	Reference output voltage	V_{O}
	TJA1040 TIMING SECTION	
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
$t_{PD(TXD–RXD)}$	Prop delay TXD to RXD	Device t_{LOOP1} and t_{LOOP2}
$t_{d(stb-norm)}$	Enable time from standby to dominant	Driver t_{en}
	TJA1040 STB PIN SECTION	
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1040 Product Specification, Philips Semiconductors, 2003 February 19.

Equivalent Input and Output Schematic Diagrams



TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

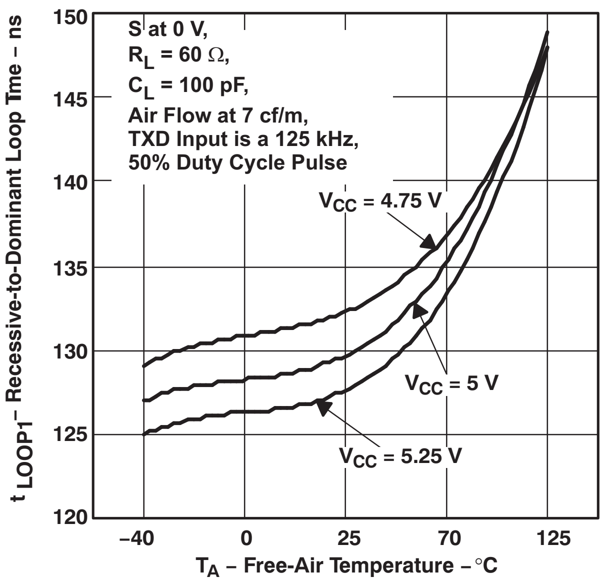


Figure 14.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

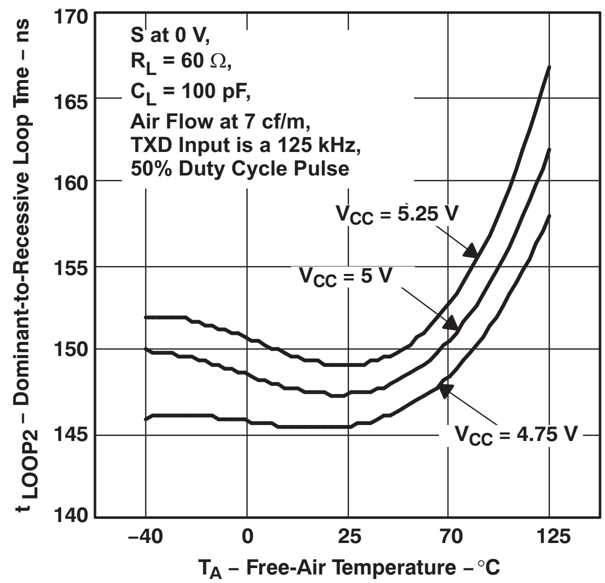


Figure 15.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE

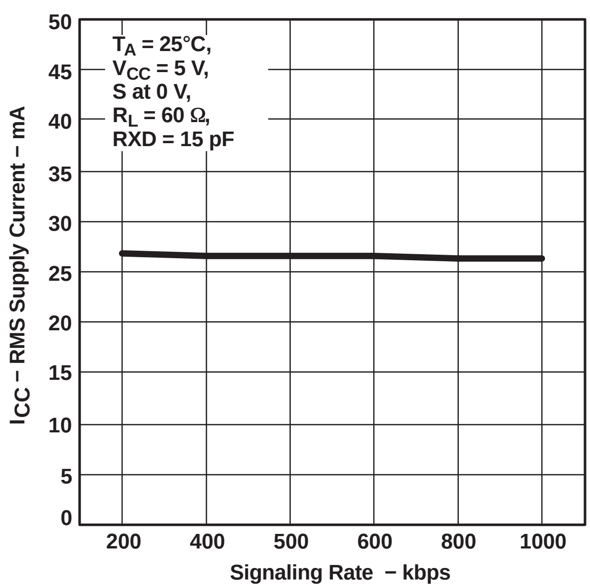


Figure 16.

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

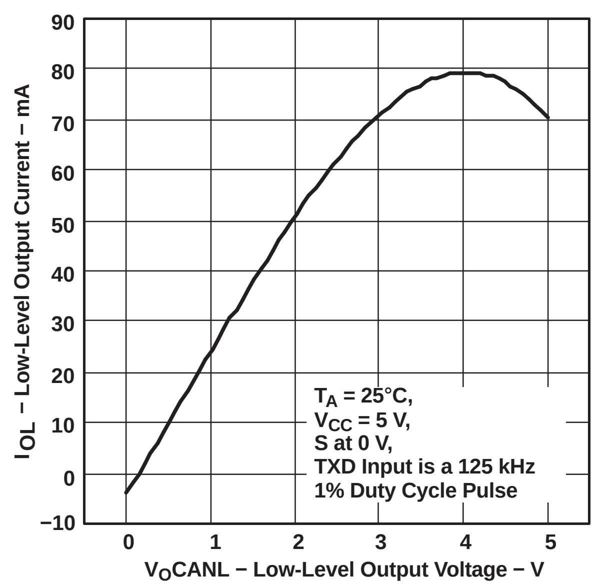


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

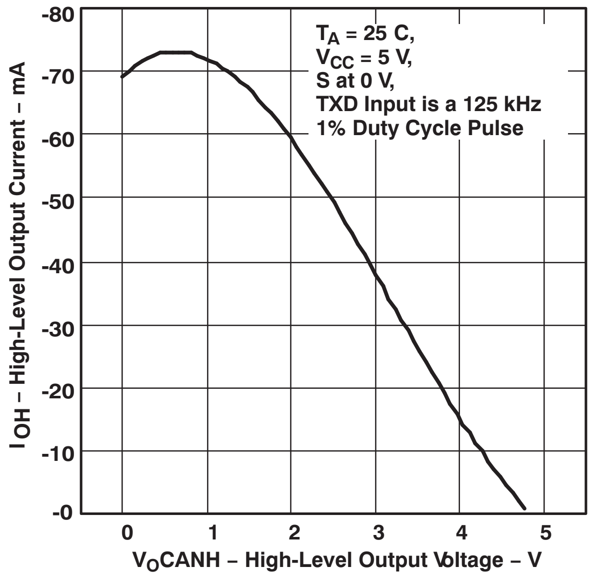


Figure 18.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE (across V_{CC})

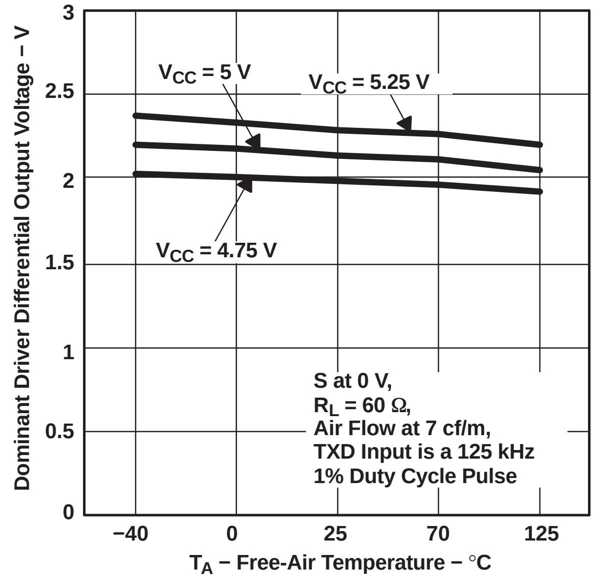


Figure 19.

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

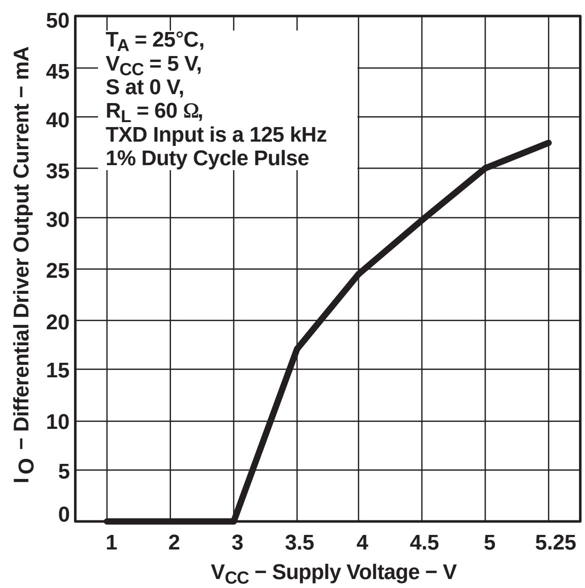


Figure 20.

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

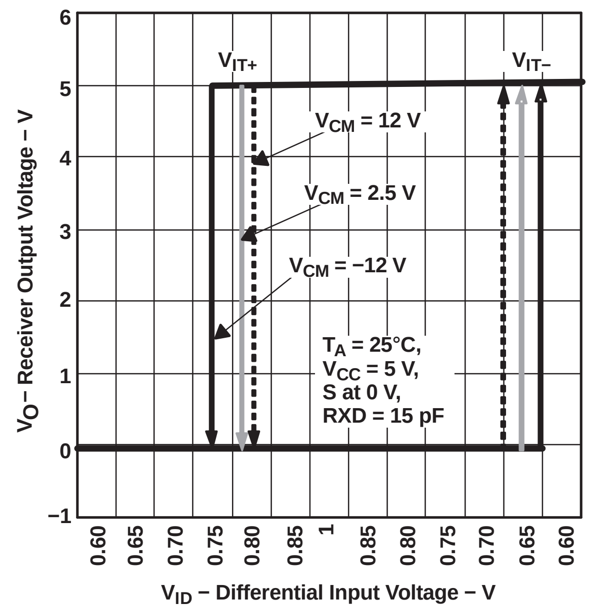


Figure 21.

TYPICAL CHARACTERISTICS (continued)

TYPICAL ELECTROMAGNETIC EMISSIONS UP TO 50 MHZ (Peak Amplitude)

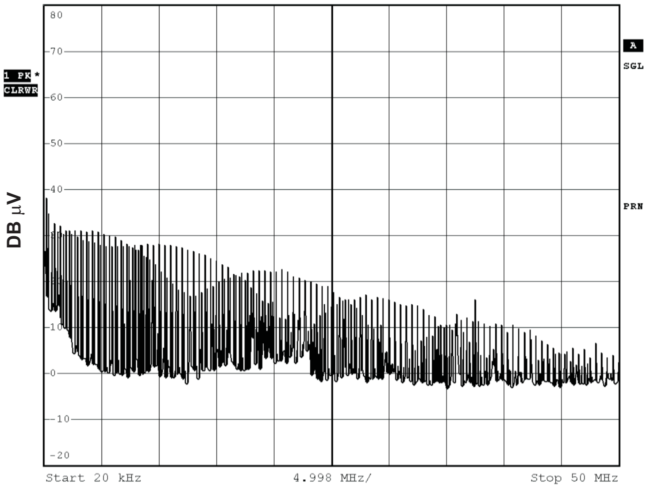


Figure 22. Frequency Spectrum of Common-Mode Emissions

TYPICAL ELECTROMAGNETIC IMMUNITY PERFORMANCE

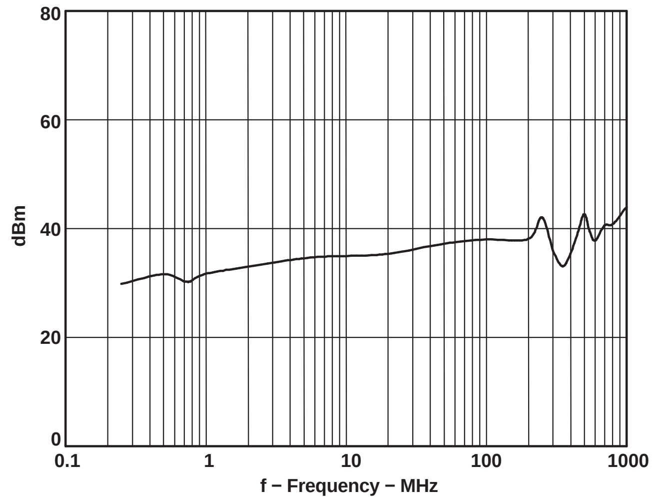


Figure 23. Direct Power Injection (DPI) Response vs Frequency

APPLICATION INFORMATION

CAN Basics

The basics of arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this “sample” is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the approximately 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system also need to be accounted for with adjustments in signaling rate and stub and bus length. Table 5 lists the maximum signaling rates achieved with the SN65HVD1040 with several bus lengths of category 5, shielded twisted pair (CAT 5 STP) cable.

Table 5. Maximum Signaling Rates for Various Cable Lengths

Bus Length (m)	Signaling Rate (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

The ISO 11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A large number of nodes requires a transceiver with high input impedance such as the HVD1040.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the standard should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard’s –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity. The HVD1040 enhances the Standard’s insurance of data integrity with an extended –12 V to 12 V range of common-mode operation.

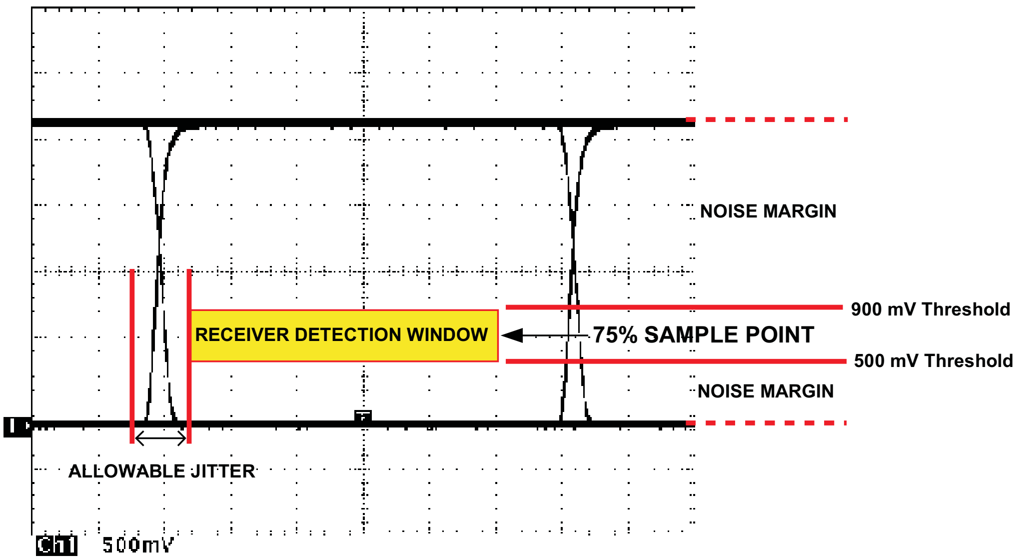


Figure 24. Typical CAN Differential Signal Eye-Pattern

An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 25, the differential signal changes logic states in two places on the display, producing an "eye." Instead of viewing only one logic crossing on the scope, an entire "bit" of data is brought into view. The resulting eye pattern includes all of the effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900 mV or 500 mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces and cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects, V_{CC} and ground bounce, and electromagnetic interference from near-by electrical equipment.

The balanced receiver inputs of the HVD1040 mitigate most all sources of signal corruption, and when used with a quality shielded twisted-pair cable, help insure data integrity.

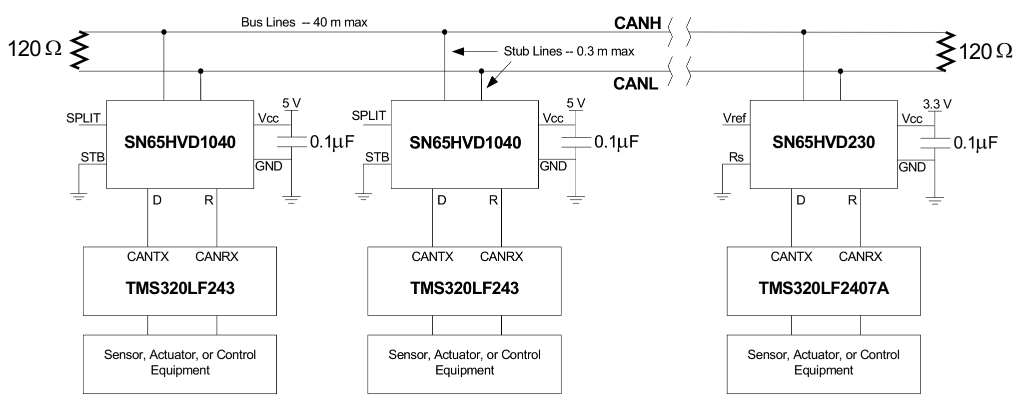


Figure 25. Typical HVD1040 Application

Thermal Shutdown

The SN65HVD1040 has a thermal shutdown that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions, and not exceed absolute maximum ratings at all times. If the SN65HVD1040 is subjected to many or long durations faults that can put the device into thermal shutdown, it should be replaced.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65HVD1040D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1040DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1040DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1040DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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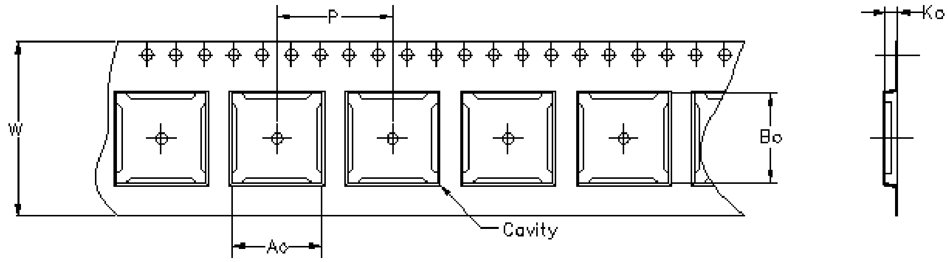
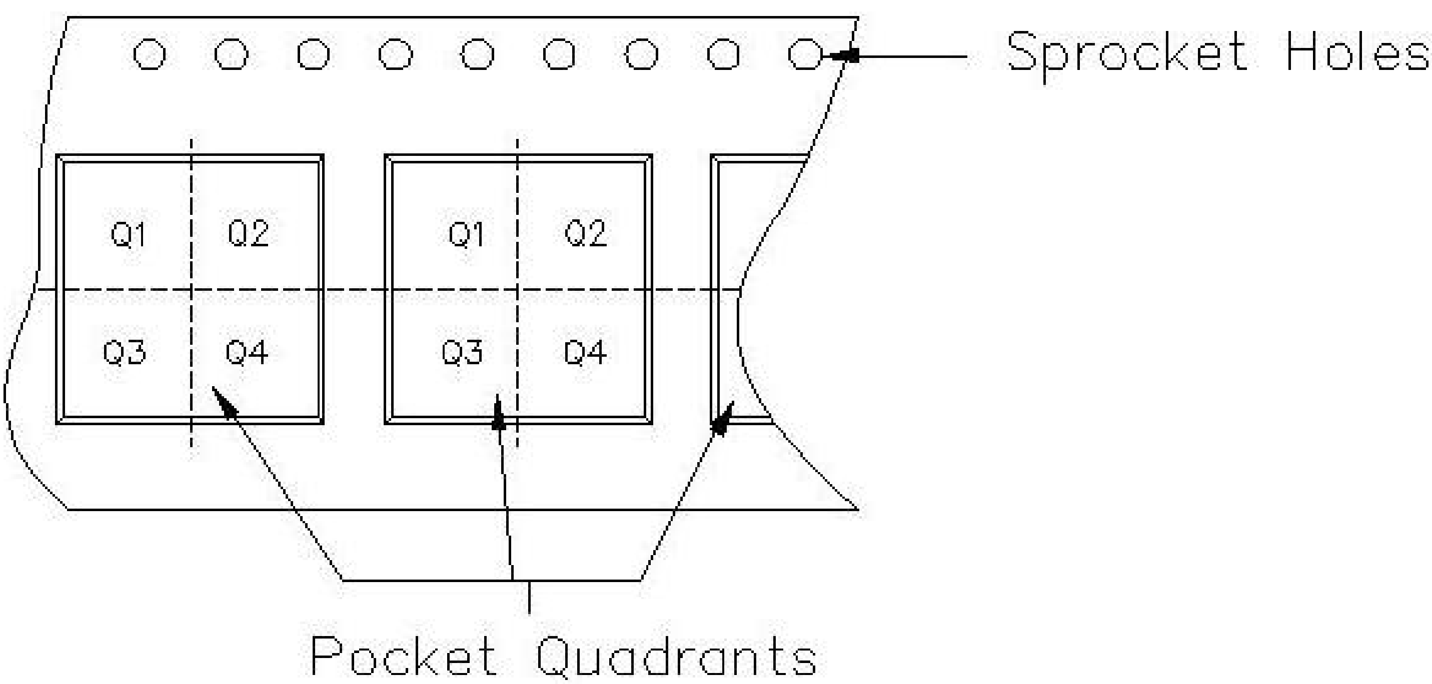


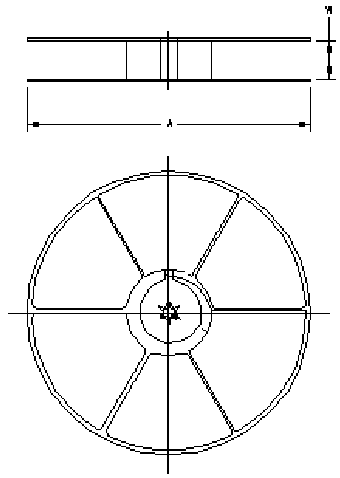
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.



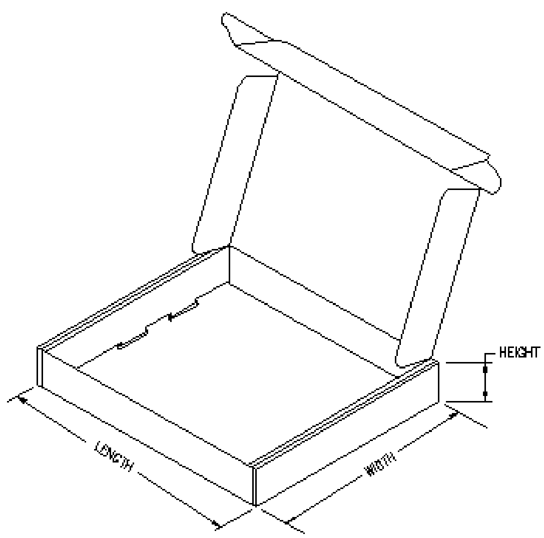
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1040DR	D	8	TAI	330	12	6.4	5.2	2.1	8	12	PKGORNT1TR-MSP

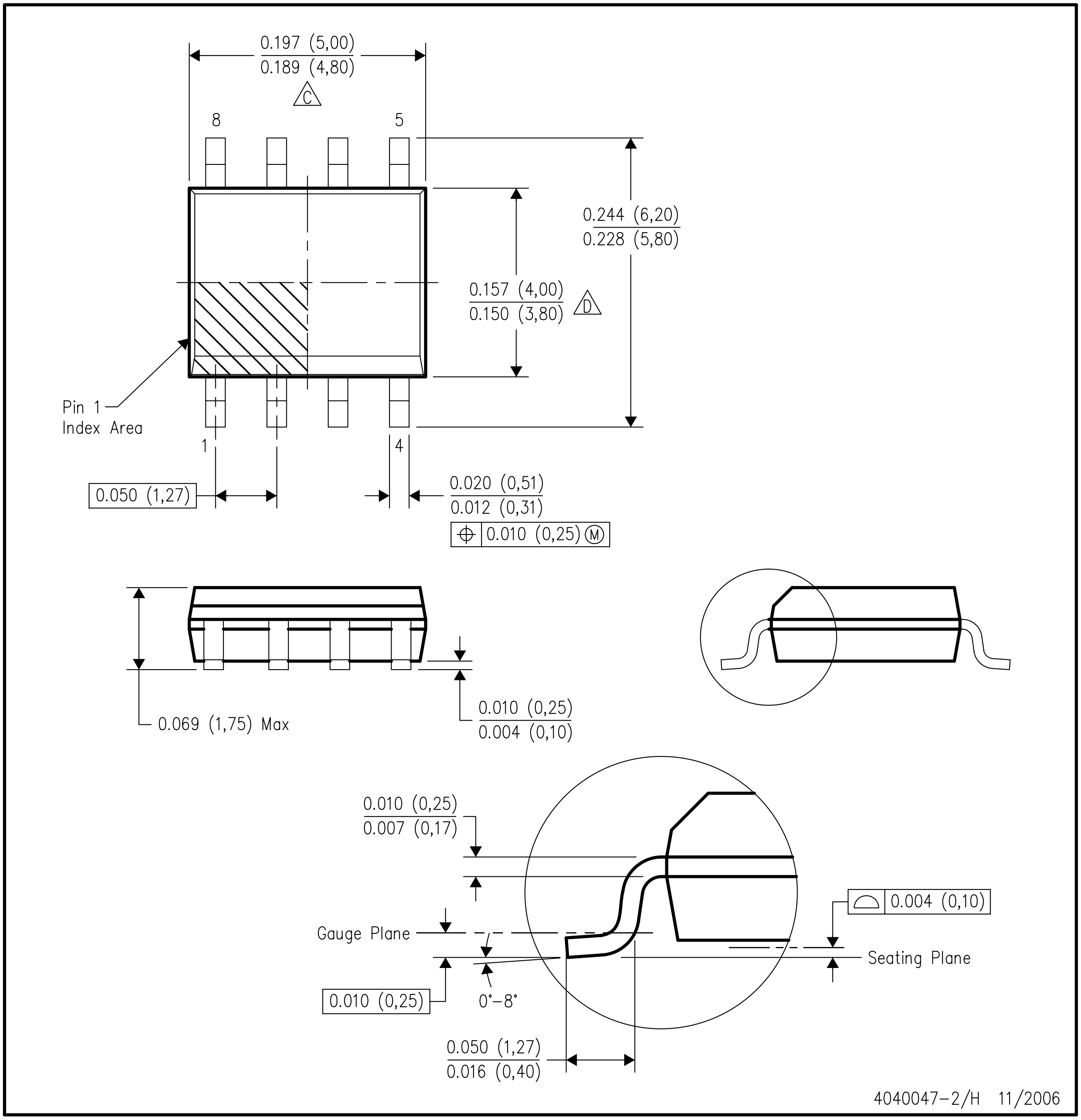


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65HVD1040DR	D	8	TAI	346.0	346.0	29.0



D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.